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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,560	ZIMMERMANN, KLAUS	
	Examiner	Art Unit	
	Andrew C. Lee	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/07/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Regarding Fig. 3, pages 8 - 9, the subject matters "input controller, output controller"; computer-readable medium as disclosed in claim 41. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- Page 7, line 29 – 32, and Page 8 lines 1 – 5, the applicants discloses that "In the FIG. 2 embodiment, memory 120 preferably includes, but is not limited to, an input controller 212, an output controller 214, a video decoder 216, an audio decoder 218, a video output module 220, an audio output module 222, a demultiplexer (demux) module 224, video decode timestamps 226, audio

decode timestamps 228, video output timestamps 230, audio output timestamps 232, video buffers 234, and audio buffers 236.

In alternate embodiments, memory 120 may readily include various other components in addition to, or instead of, those components discussed in conjunction with the FIG. 2 embodiment. The functionality and utilization of the foregoing components of memory 120 are further discussed below in conjunction with FIGS. 3 through 8"." The Office would like Applicant to provide more clarification on these issues. It is not clear how memory 120 as disclosed in Fig. 3 relating to an input controller 212, an output controller 214, a video decoder 216, an audio decoder 218, a video output module 220, an audio output module 222, a demultiplexer (demux) module.....etc. Does the memory just provide temporary storage function for the bitstreams for the subject matters of input controller 212, an output controller 214, a video decoder 216, an audio decoder 218, a video output module 220, an audio output module 222, a demultiplexer (demux) module. Or these subject matters are physical interfaces in the disclosure related to Fig. 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1- 4, 6 – 10, 12 – 24, 26 – 30, 32 – 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada et al.(U.S. 5668601).

Regarding claims 1, 21, 42, 43, Okada et al. discloses the limitation of a system, method for performing a data synchronization procedure (Abstract, lines 1 – 3; column 19, claim 1), comprising: a demultiplexer configured to recover elementary bitstreams, and to extract decode timestamps and output timestamps corresponding to said elementary bitstreams (Abstract, lines 3 – 7; column 19, claim 1); one or more decoders configured to decode said elementary bitstreams to produce decoded frames (Abstract, lines 7 – 14; column 19, claim 1); an input controller configured to control said one or more decoders according to said decode timestamps (Fig.1, elements 14, 24; column 19, claim 1); one or more output modules configured to process said decoded frames to produce processed frames (column 4, lines 49 – 56); and an output controller configured to control said one or more output modules according to said output timestamps, said output controller performing an output timing resynchronization procedure to align output frame timings of said processed frames according to said output timestamps (column 6, lines 7 – 36).

Regarding claims 2, 22, Okada et al. discloses the limitation of the system, method of claimed wherein said data synchronization procedure is performed by a

receiver device that receives a multiplexed bitstream from a data source and responsively generates said processed frames to one or more destination devices (Abstract, lines 1 – 14; column 4, lines 57 – 59).

Regarding claims 3, 23, Okada et al. discloses the limitation of the system, method of claimed wherein said one or more elementary bitstreams include a video bitstream and an audio bitstream, said one or more decoders including a video decoder and an audio decoder, said one or more output modules including a video output module and an audio output module (column 4, lines 49 – 56).

Regarding claims 4, 24, Okada et al. discloses the limitation of the system, method of claimed wherein said input controller and said output controller are decoupled to operate independently, and wherein said receiver handles said video bitstream and said audio bitstream independently by utilizing a plurality of different timebases (column 6, lines 7 – 36; column 5, lines 1 – 4).

Regarding claims 6, 26, Okada et al. discloses the limitation of the system, method of claimed wherein said video decoder accesses said video bitstream from a video decoder buffer and stores decoded video frames into a video output buffer, said video output module accessing said decoded video frames from said video output buffer (column 21, claim 21), said audio decoder accessing said audio bitstream from an audio decoder buffer and storing decoded audio frames into an audio output buffer, said audio

output module accessing said decoded audio frames from said audio output buffer (column 21, claim 21).

Regarding claims 7, 27, Okada et al. discloses the limitation of the system, method of claimed wherein said demultiplexer separates a composite bitstream into said elementary bitstreams, said decode timestamps including video decode timestamps and audio decode timestamps, said output timestamps including video output timestamps and audio output timestamps (Abstract, lines 7 – 14; column 8, lines 9 – 13).

Regarding claims 8, 28, Okada et al. discloses the limitation of the system, method of claimed wherein said input controller instructs said video decoder to generate a decoded video frame when a corresponding one of said video decode timestamps equals a receiver system time clock (column 19, claim 2, column 20, lines 20 – 26), said input controller also instructing said audio decoder to generate a decoded audio frame when a corresponding one of said audio decode timestamps equals a receiver system time clock (column 19, claim 2, column 20, lines 9 – 15).

Regarding claims 9, 29, Okada et al. discloses the limitation of the system, method of claimed wherein said output controller instructs said video output module to output a processed video frame when a corresponding one of said video output timestamps equals a receiver system time clock (column 19, claim 5, column 20, lines 62 – 65), said output controller also instructing said audio output module to output a

processed audio frame when a corresponding one of said audio output timestamps equals a receiver system time clock (column 19, claim 5, column 20, lines 56 – 59).

Regarding claims 10, 30, Okada et al. discloses the limitation of the system, method of claimed wherein said receiver device generates a series of decoded video frames, said receiver device also generating a series of decoded audio frames, said receiver device subsequently outputting a series of processed video frames corresponding to said decoded video frames, said receiver device also subsequently outputting a series of processed audio frames corresponding to said decoded audio frames (column 4, lines 37 – 42).

Regarding claims 12, 32, Okada et al. discloses the limitation of the system, method of claimed wherein said demultiplexer separates a composite bitstream into said elementary bitstreams, said decode timestamps including new decode timestamps, said output timestamps including new output timestamps (column 2, lines 59 – 61; column 4, lines 37 – 42; column 7, lines 35 – 67).

Regarding claims 13, 33, Okada et al. discloses the limitation of the system, method of claimed wherein said input controller instructs said one or more decoders to generate one of said decoded frames when a corresponding one of said new decode timestamps equals a receiver system time clock (column 7, lines 53 – 58).

Regarding claims 14, 34, Okada et al. discloses the limitation of the system of claimed wherein said one or more decoders store said one of said decoded frames into a buffer memory for said one or more output modules to access (column 7, lines 45 – 50).

Regarding claims 15, 35, Okada et al. discloses the limitation of the system, method of claimed wherein said receiver device generates a series of decoded frames, said receiver device subsequently outputting a series of processed frames corresponding to said decoded frames (column 7, lines 45 – 50).

Regarding claims 16, 36, Okada et al. discloses the limitation of the system, method of claimed wherein said output controller determines whether said output frame timings of said processed frames are aligned with said new output timestamps (column 14, lines 1 – 11).

Regarding claims 17, 37, Okada et al. discloses the limitation of the system , method of claimed wherein said output controller performs said output timing resynchronization procedure to align said output frame timings of said processed frames with said new output timestamps (column 14, lines 12 – 31).

Regarding claims 18, 38, Okada et al. discloses the limitation of the system, method of claimed wherein said output controller instructs said one or more output

modules to sequentially output one of said processed frames when a corresponding one of said new output timestamps equals a receiver system time clock (column 31 – 38).

Regarding claims 19, 39, Okada et al. discloses the limitation of the system, method of claimed wherein said receiver device outputs a series of processed frames corresponding to said decoded frames (column 19, claim 1).

Regarding claims 20, 40, Okada et al. discloses the limitation of the system, method of claimed wherein said receiver device outputs said series of processed video frames to a video display device, said receiver device also outputting said series of processed audio frames to an audio reproduction system (Fig. 1, elements 25, 26, 27; column 8, lines 5 – 7).

Regarding claim 41, Okada et al. discloses the limitation of a computer-readable medium comprising program instructions (column 3, lines 23 – 34) for performing a data synchronization procedure (Abstract, lines 1 – 3; column 19), claimed by performing the steps of: recovering elementary bitstreams with a demultiplexer that also extracts decode timestamps and output timestamps corresponding to said elementary bitstreams (Abstract, lines 3 – 7; column 19, claim 1); decoding said elementary bitstreams with one or more decoders to produce decoded frames (Abstract, lines 7 – 14; column 19, claim 1); controlling said one or more decoders according to said decode timestamps by utilizing an input controller (Fig.1, elements 14, 24; column 19, claim 1); processing said decoded

frames with one or more output modules to produce processed frames (column 4, lines 49 – 56); and controlling said one or more output modules according to said output timestamps by utilizing an output controller that performs an output timing resynchronization procedure to align output frame timings of said processed frames according to said output timestamps (column 6, lines 7 – 36).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 11, 25, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. (U.S. 5668601) in view of Lee (U.S. 6236432 B1).

Regarding claims 5, 25, Okada et al. discloses the limitation of the system of claimed wherein said output timing resynchronization procedure is performed after receiving new output timestamps (column 14, lines 7 – 11). Okada et al. does not disclose expressly the limitation of as a result of at least one of a program change event, a bitstream discontinuity, and a powerup initialization event. Lee discloses the limitation of as a result of at least one of a program change event, a bitstream discontinuity, and a powerup initialization event (column 4, lines 35 – 67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okada et al. to

include a as a result of at least one of a program change event, a bitstream discontinuity, and a powerup initialization event such as that taught by Lee in order to provide an MPEG II system with a PES decoder, in which a software basic program stream and a hardware basis transport stream are demultiplexed irrespective of forms of the streams for restoring a video signal and an audio signal (as suggested by Lee, see column 1, lines 6 – 10).

Regarding claims 11, 31, Okada et al. discloses the limitation of a system for performing a data synchronization procedure (Abstract, lines 1 – 3; column 19, claim 1), Okada et al. does not disclose expressly the system of claimed wherein a system user instructs said receiver device to select a new program, said receiver device responsively performing a program search procedure to locate said new program. Lee discloses the limitation of the system of claimed wherein a system user instructs said receiver device to select a new program, said receiver device responsively performing a program search procedure to locate said new program (column 4, lines 35 – 48; lines 59 – 67; column 6, lines 33 – 56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okada et al. to include a system of claimed wherein a system user instructs said receiver device to select a new program, said receiver device responsively performing a program search procedure to locate said new such as that taught by Lee in order to provide an MPEG II system with a PES decoder, in which a software basic program stream and a hardware basis transport stream are demultiplexed

irrespective of forms of the streams for restoring a video signal and an audio signal (as suggested by Lee, see column 1, lines 6 – 10).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ACL Aug 28, 2005

Ajit Patel
Primary Examiner